HIGH-PERFORMANCE ONE-TRANSISTOR MEMORY CELL

Abstract of the Disclosure

One aspect of this disclosure relates to a memory cell. In various embodiments, the memory cell includes an access transistor having a floating node, and a diode connected between the floating node and a diode reference potential line. The diode includes an anode, a cathode, and an intrinsic region between the anode and the cathode. A charge representative of a memory state of the memory cell is held across the intrinsic region of the diode. In various embodiments, the memory cell is implemented in bulk semiconductor technology. In various embodiments, the memory cell is implemented in semiconductor-on-insulator technology. In various embodiments, the diode is gate-controlled. In various embodiments, the diode is charge enhanced by an intentionally generated charge in a floating body of an SOI access transistor. Various embodiments include laterally-oriented diodes (stacked and planar configurations), and various embodiments include vertically-oriented diodes. Other aspects and embodiments are provided herein.